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TITLE: METHOD FOR FORMING AND REMOVING SELECTIVE GROWTH MASK

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ABSTRACT:

PURPOSE: To provide a method for forming and removing a selective growth mask which can be employed in a vacuum through process while suppressing the
adverse effect on the crystallinity and exhibiting required resistance against any type of material gas.

CONSTITUTION: The temperature of a GaAs substrate 201 is set to 630°C
and a Ga rich surface is provided on a GaAs butter layer 202. Dimethy hydrazine is then introduced thus depositing a GaN film 203 on the surface of

the GaAs butter layer. The GaAs substrate is placed in an oxygen atmosphere and the surface of the GaN film is irradiated with the light from a halogen lamp thus forming a GaO1-xNx 204. Subsequently, the surface of GaO1-xNx is irradiated with chloride gas and scanned by means of an electron beam. Consequently, the GaO1-xNx and GaN film are removed from the region scanned by
the electron beam and serve as a mask for selective growth in other regions.

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DISCLOSURE TEXT:

2p. In order to study the electrochemistry of additive plating techniques, such as those used in the fabrication of magnetic bubble devices, it is necessary to place a reference electrode as close as possible to the actual plating surface. This must be accomplished without disturbing the electro-chemical environment of the cell in any manner. When studying electrodeposition through a fine-line resist mask, this becomes extremely difficult. Until now, this ideal situation could be approximated at best. To solve this problem, a process is described for fabricating samples which will allow the observation of cathode potentials at the actual plating surface within individual device elements of the smallest dimensions.

- These samples are formed by applying a layer 6 of a suitable resist to a wafer 4 of a metal such as copper. The desired device pattern is written on the wafer with a vector scan electron beam system to expose regions 8. A particular feature of the device is chosen, and the electron beam is directed to its location (i.e., regions 8). A portion of this feature is then re-exposed, creating an over-exposed area 10 within it (Fig. 1). The wafer is developed to the point at which this small area 10 is opened while the balance of the structure remains undeveloped. Next, the wafer is etched to form a microscopic pinhole 12 through the wafer (Fig. 2). The sample is then completely developed to form the complete resist stencil

(Fig. 3).

- At this point the sample is ready for use, and can be placed in the cell for plating onto surface 14. The reference electrode can be connected to the capillary pinhole 12 using the plating bath as the connecting electrolyte.

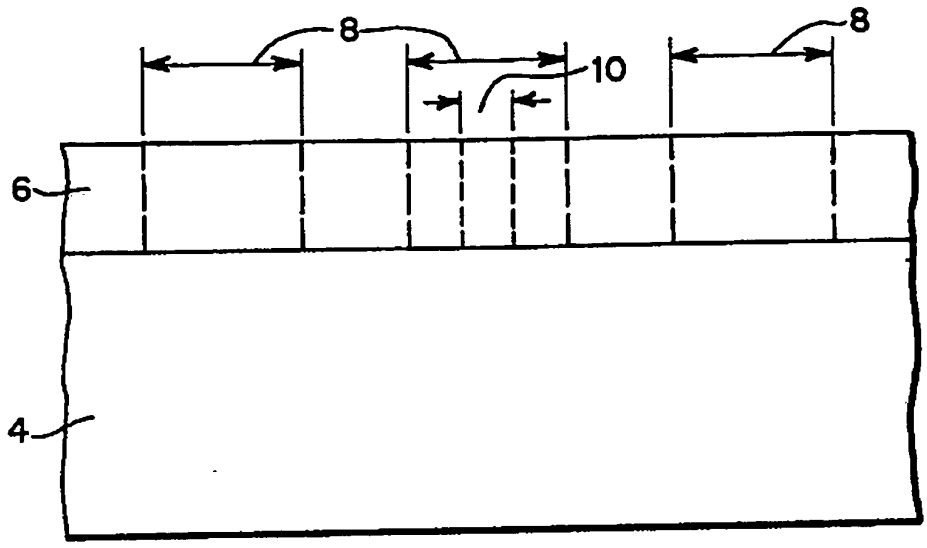

FIG. 1

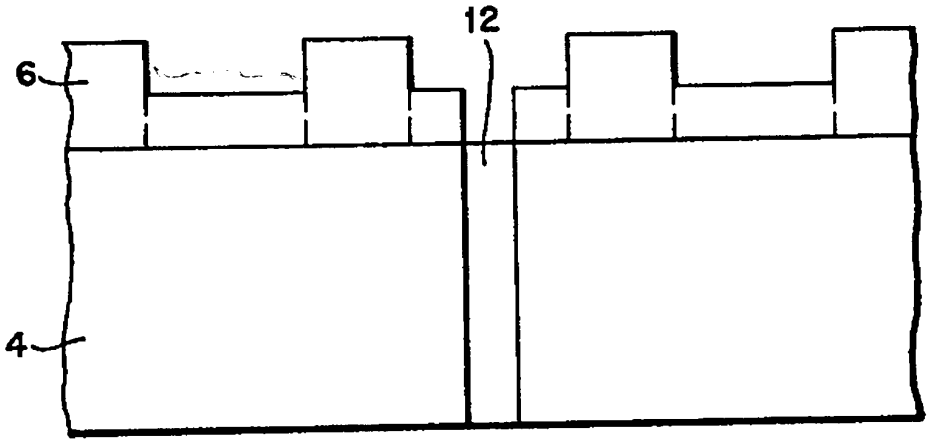

FIG. 2

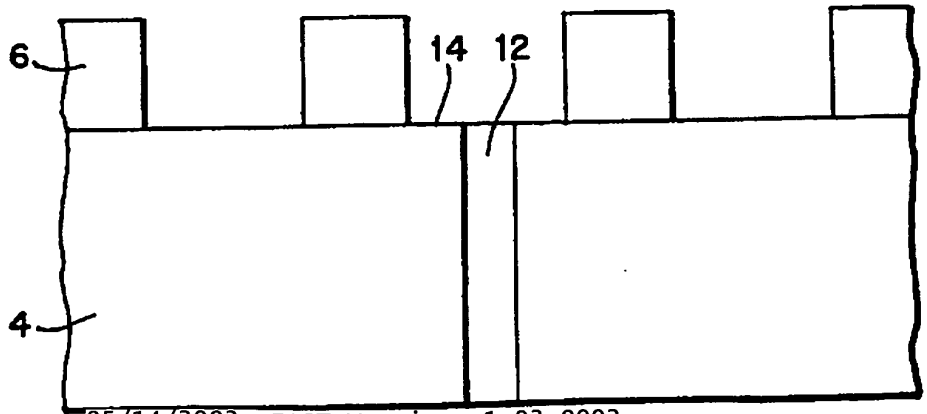

FIG. 3